CLAIMS

1. An electronic semiconductor device, comprising:

a body of semiconductor material having an upper surface;

a dielectric layer extending on top of said body; and

a contact structure in said dielectric layer, said contact structure comprising a first conducting region and a second conducting region, said second conducting region being of chalcogenic material and being in electric contact with said first conducting region;

wherein said first conducting region has a strip-like shape having a longitudinal direction delimited by an end face extending transversely to said upper surface and forming a contact area with said second conducting region.

2. A device according to claim 1 wherein said first conducting region extends in a direction parallel to said upper surface.

3. A device according to claim 1 wherein said end face is perpendicular to said upper surface within process tolerances.

4. A device according to claim 1 wherein said end face has a generally rectangular shape having a height and a width.

5. A device according to claim 4 wherein said height is comprised between 5 nm and 50 nm and said width is comprised between 5 nm and 50 nm.

6. A device according to claim 1, wherein the contact structure is part of a PCM storage element of a PCM memory cell that further includes a selection element, said storage element being formed by a heater element including said first conducting region and a storage region comprising said second conducting region.

7. A device according to claim 6 wherein said selection element is formed in said body, a lower electrode extends in said dielectric layer between said selection element and said first conducting region and an upper electrode extends in said dielectric layer on said second conducting region and forms a bit line.

8. A device according to claim 7 wherein said second conducting region has a reduced area portion in contact with said first conducting region and an upper enlarged portion extending on top of said reduced area portion and in contact with said upper electrode.

9. A process for manufacturing an electronic semiconductor device, comprising the steps of:

providing a body of semiconductor material having an upper surface;

forming a dielectric layer extending on top of said body; and

forming a contact structure in said dielectric layer, said step of forming a contact structure comprising forming a first conducting region and forming a second conducting region of chalcogenic material in electric contact with said first conducting region;

wherein said step of forming said first conducting region comprises forming a strip-shaped region having a longitudinal direction delimited by an end face extending transversely to said upper surface;

and said step of forming a second conducting region comprises forming said second conducting region in contact with said first conducting region at said end face.

10. A process according to claim 9 wherein said end face has a generally rectangular shape having a height comprised between 5 nm and 50 nm and a width comprised between 5 nm and 50 nm.

11. A process according to claim 9 wherein said step of forming said first conducting region comprises depositing a first conductive layer on a bottom portion of said dielectric layer; forming a delimitation layer on top of said first conductive layer, said delimitation layer having a step with a vertical side wall surface; forming a sacrificial portion on said vertical side wall surface; removing said first delimitation layer; etching said first conductive layer using said a sacrificial portion as a mask; and removing said sacrificial portion.

12. A process according to claim 11 wherein said step of forming a sacrificial portion comprises depositing a sacrificial layer on said first conducting region and said delimitation layer and anisotropically etching said sacrificial layer.

13. A process according to claim 11 wherein after removing said sacrificial portion, an insulating layer is deposited on said first conducting region and said bottom portion of said dielectric layer; a trench is formed to remove at least a portion of said bottom portion and an end portion of said first conducting region, thereby defining said end face; and a second conductive layer of said chalcogenic material is deposited, filling said trench and contacting said end face.

14. A process according to claim 13, comprising the step of forming a PCM device including a memory cell comprising a selection element and a storage element, said storage element being formed by a heater element including said first conducting region and a storage region comprising said second conducting region.

15. A process according to claim 14, comprising, after depositing said second conductive layer, depositing an electrode layer and defining said electrode layer and said second conductive layer, to define a bit line.

16. An electronic PCM device, comprising:

a body of semiconductor material having lower surface;

a dielectric layer extending on top of the body; and

a PCM memory cell that includes a PCM storage element formed in the dielectric layer and a selection element, the storage element being formed by a heater element and a storage region, the storage region being of chalcogenic material and being in electric contact with the heater element, wherein the heater element has an end face extending transversely to the lower surface and forming a contact area with the storage region.

17. The PCM device of claim 16 wherein the heater element extends longitudinally in a direction parallel to the lower surface.

18. The PCM device of claim 16 wherein the end face is perpendicular to the lower surface within process tolerances.

19. The PCM device of claim 16 wherein the end face has a generally rectangular shape having a height and a width.

20. The PCM device of claim 19 wherein the height is comprised between 5 nm and 50 nm and the width is comprised between 5 nm and 50 nm.

21. The PCM device of claim 16 wherein the selection element is formed in the body, a lower electrode extends in the dielectric layer between the selection element and the heater element and an upper electrode extends in the dielectric layer on the storage region and forms a bit line.

22. The PCM device of claim 21 wherein the storage region has a reduced area portion in contact with the heater element and an upper enlarged portion extending on top of the reduced area portion and in contact with the upper electrode.